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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 003771.P001D Total Pages 5

First Named Inventor or Application Identifier Daniel E. Grupp

Express Mail Label No. EL627467566US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [x] Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)

2. [x] Specification (Total Pages 22)
   (preferred arrangement set forth below)
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure

3. [x] Drawings(s) (35 USC 113) (Total Sheets 5)

4. [x] Oath or Declaration (Total Pages 4)
   a. [ ] Newly Executed (Original or Copy)
   b. [X] Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. [ ] DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [X] Incorporation By Reference (useable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. __X__ a. Information Disclosure Statement (IDS)/PTO-1449
__X__ b. Copies of IDS Citations
12. __X__ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
_____ b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
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17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation __X__ Divisional ____ Continuation-in-part (CIP)
of prior application No: 09/296,858

18. **Correspondence Address**
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or
__X__ Correspondence Address Below

NAME Tarek N. Fahmi – Reg. No.: 41,402
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
ADDRESS 12400 Wilshire Boulevard
Seventh Floor
CITY Los Angeles STATE California ZIP CODE 90025-1026
Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

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Serial/Patent No.: ***
Client: Acorn Technologies
Filing/Issue Date: Herewith
Title: ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR

BSTZ File No.: 003771.P001D
Date Mailed: 7/7/2000
Atty/Secty Initials: TNF/pab/tj
Docket Due Date:

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

- ☐ Amendment/Response (____ pgs.)
- ☐ Appeal Brief (____ pgs.) (in triplicate)
- ☐ Application - Utility (____ pgs., with cover and abstract)
- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
- ☒ Application - Rule 1.53(b) Divisional (22 pgs.)
- ☐ Application - Rule 1.53(b) CIP (____ pgs.)
- ☐ Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- ☐ Application - Design (____ pgs.)
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- ☐ Disclosure Docs & Orig & Copy of Inventors Signed Letter (____ pgs)
- ☒ Drawings: 5 # of sheets includes 9 figures

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

DANIEL E. GRUPP

Application No: Not Yet Assigned

Filed: Herewith

For: ELECTRONSTATICALLY OPERATED TUNNELING TRANSISTOR

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

A Divisional of:

Serial No.: 09/296,858

Filed: April 22, 1999

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicant respectfully requests that the above-identified application be preliminarily amended as follows:

IN THE CLAIMS:

Please cancel claim 1-22 without prejudice.

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09296858 - 070700

REMARKS

This application is being filed as a divisional of application serial number 09/296,858, filed on April 22, 1999, in which a restriction requirement was mailed on June 13, 2000. Claims pending in the instant application are numbered 23-25. The Applicant respectfully requests consideration of the instant divisional application as amended.

If there are any additional fees, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 7/7/2000

Tarek N. Fahmi
Reg. No. 41,402

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

09296858 - 042200

003771.P001 Patent

United States Patent Application

For

ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR

Inventor:

Daniel E. Grupp

Prepared by:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026
(408) 720-8598

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Electrostatically Operated Tunneling Transistor

FIELD OF THE INVENTION

This invention relates generally to solid state switching and amplification devices, i.e. transistors. More particularly, it relates to tunneling transistor devices having tunnel junctions.

BACKGROUND

Complementary metal oxide semiconductor (CMOS) devices such as MOSFET transistors are commonly used in high speed, highly integrated circuits. Integrated circuit manufacturers are constantly increasing the operating speed and decreasing the size of MOSFET transistors. Such improvements yield smaller, faster ICs with more functions at lower cost.

Various problems exist with scaling MOSFET devices below 0.1 microns, however. For example, with channel lengths less than 0.1 microns the required channel doping levels become very high. It is difficult to produce high doping levels with high uniformity over the surface of a wafer. Therefore, different MOSFETs manufactured on the same wafer will have very different characteristics if high doping levels are used. Also, capacitive coupling between drain and source regions of individual MOSFETs becomes significant. Problems also exist in mass producing such devices.

For these reasons, researchers have been investigating transistor devices based on the quantum behavior of electrons in very small devices. A number of such devices that exploit electron tunneling are known in the art.

For example, U.S. Patent 5,705,827 to Baba et al. discloses a tunneling transistor device having an insulated gate. The transistor operation is provided by band bending in a current

channel adjacent to the gate electrode, as in a MOSFET device. The drain electrode forms an Esaki tunnel junction with the current channel.

U.S. Patent 4,675,711 to Harder et al. discloses a tunneling transistor using an insulated gate electrode disposed adjacent to a tunneling layer. The tunneling layer has a band gap energy different from that of semiconductor source and drain contacts. A voltage applied to the gate changes an energy barrier height of the tunneling layer, thereby controlling a tunnel current through the tunnel layer. The device must be operated at low temperature so that thermally excited carriers do not provide conduction through the tunnel layer.

U.S. Patent 5,834,793 to Shibata discloses a tunneling MOSFET transistor device having an insulated gate contact. Adjacent to the gate contact is a short current channel. Source and drain contacts are separated from the current channel by dielectric tunnel barriers about 30 Angstroms thick. The device exhibits negative resistance characteristics due to discrete energy states in the current channel.

U.S. Patent 5,291,274 to Tamura discloses a tunneling transistor. The transistor of Tamura has a middle layer high dielectric constant material disposed between two tunnel junctions. The middle layer is in direct contact with a gate electrode. Source and drain electrodes are provided in contact with the tunnel junctions. When a voltage is applied to the gate electrode, the electrical potential of the middle layer is changed, thereby allowing electrons to tunnel between source and drain. A problem with the device of Tamura is that current will flow to and from the gate electrode when the device is on. Therefore, the device of Tamura requires continuous gate current for continuous operation. This is highly undesirable in many applications.

In addition to the above, others have investigated the uses of single electron transistors having tunneling junctions. A single electron transistor has a very small metallic or semiconductor island disposed between two tunnel junctions having a high resistance. Source and drain contacts are made to the tunnel junctions. A gate electrode capacitively coupled to

the island provides switching control. The island is made sufficiently small such that an energy required to charge the island with a single electron is greater than the thermal energy available to electrons in the source and drain contacts. The energy required to charge the island with a single electron is given by $E_C=e^2/2C$, where e is the charge of an electron, and C is the capacitance of the island. This energy requirement for charging the island is termed the Coulomb blockade.

In operation, a voltage applied to the gate electrode capacitively raises or lowers the potential of the island. When the island potential is lowered by a certain amount, electrons can tunnel through one tunnel junction onto the island, and tunnel through the other tunnel junction off of the island. In this way, current is allowed to flow through the island for certain values of gate voltage. The resistance of a single electron transistor exhibits oscillations as gate voltage changes monotonically.

Available thermal energy increases with temperature, of course, so a single electron transistor has a maximum temperature at which it can be operated. The maximum operating temperature is determined by the capacitance of the island, which is a function of the island size. For devices to operate at room temperature, the capacitance C must be less than about 10 Attofarads. Realizing such low capacitance requires that the island be very small (e.g., less than 10 nm on a side) and located relatively far from the source, drain and gate. It is very difficult to make a single electron transistor which operates at room temperature.

An important concern in the design of a single electron transistor is the resistance of the tunnel junctions. It is best for a single electron transistor to have tunnel junctions with relatively high resistances (i.e., much greater than a quantum resistance $R_q = h/2e^2 \approx 26$ KOhms, where h is Planck's constant). If the resistance of the tunnel junctions is too low, then the number of electrons on the island is not well defined. Operation of a single electron transistor requires that the tunnel junctions have sufficiently high resistances such that electron locations are well defined as being either in the island or outside the island.

However, high tunnel junction resistance results in a high resistance between source and drain contacts, even in a fully 'ON' state. A high resistance limits the switching speed and increases the power consumption of the device. Therefore, single electron transistors are limited in their electrical characteristics and potential applications.

A distinguishing characteristic of single electron transistor devices is that the island can be made of semiconductor material or metal. The island does not need to be made of material having an electron energy band gap.

SUMMARY OF THE INVENTION

Disclosed herein is a transistor that includes a pair of tunnel junctions (or barriers), each having a resistance less than or equal to approximately a quantum resistance. The tunnel junctions are separated from one another by an island formed of a material having a non-uniform density of energy states (e.g., at least one region that contains available energy states adjacent to at least one region that does not contain any available energy states). The tunnel junctions are each disposed between a respective one of a pair of conductors (e.g., source and drain conductors) and the island, and a gate electrode is capacitively coupled to the island.

In some cases, the island may be formed of a semiconductor material, for example, silicon, germanium or any other semiconductor. In other cases, a superconductor may be used. The tunnel barriers may be formed of an oxide of the material from which the conductors (and/or the gate electrode) or the island is/are made or may be formed from a different material all together. In operation, a conduction path between the tunnel junctions may be formed by shifting the energy states of the island through the application of a potential to gate electrode. A current may then be passed through the conduction path via the source and drain electrodes.

In one embodiment, an apparatus for switching electrical current has an ohmically isolated island made of material (e.g., a semiconductor material such as silicon, gemanium, etc.) having a band gap. The island is sufficiently large such that electron energy levels within the island are preferably separated by less than 100 meV. The apparatus also has a source contact and a first tunnel junction barrier located between the source contact and the island. The first tunnel junction barreir has a thickness and cross sectional area selected such that a first tunnel junction formed by the interconnection of the source contact, the first tunnel junction barrier and the island has a resistance less than a quantum resistance, i.e., less than 26 KOhms. The apparatus also has a drain contact and a second tunnel junction barrier located

between the drain contact and the island. The second tunnel junction barrier has a thickness and cross sectional area selected such that a second tunnel junction formed by the interconnection of the drain contact, the second tunnel junction barrier and the island also has a resistance less than the quantum resistance. The apparatus also has a gate electrode capacitively coupled to the island.

In some cases, the first and second tunnel junctions may have resistances less than 10 KOhms. Further, in other embodiments the first and second tunnel junctions may have resistances less than 1 KOhm or even less than 100 Ohms.

The first and second tunnel junction barriers may be made of an insulating material, such as silicon dioxide or aluminum oxide, and may be separated by a distance of approximately 0.2-2.0 microns.

Preferably, the apparatus includes an insulating layer disposed between the gate electrode and the island.

BRIEF DESCRIPTION OF THE DRAWINGS

The present transistor is illustrated by way of example, and not limitation, in the accompanying drawings, in which:

Figure 1 shows a transistor structure according to an embodiment of the present invention;

Figure 2 shows an energy band diagram of the device illustrated in **Figure 1**, in a particular embodiment where the island is n-doped;

Figure 3 illustrates a circuit for using the device shown in **Figure 1**;

Figure 4 shows the energy band diagram of the device illustrated in **Figure 2** with a potential applied between source and drain, and zero potential applied between gate and drain;

Figure 5 shows the energy band diagram of the device of **Figure 2** with a potential applied between source and drain sufficient for conduction;

Figure 6 shows the energy band diagram of the device of **Figure 2** with a positive potential applied to the gate with respect to the drain;

Figure 7 shows a set of I-V (current-voltage) curves for an n-type device configured in accordance with the present invention;

Figure 8 shows an embodiment of the present transistor in which the island is p-doped, i.e., a p-type' device; and

Figure 9 shows an energy band diagram for p-type device configured in accordance with the present invention with a negative gate voltage applied.

DETAILED DESCRIPTION

A switching device employing low resistance tunnel junctions is disclosed herein. More specifically, a transistor-like device having a pair of tunnel junctions, each with a resistance less than or equal to approximately the quantum resistance ($R_q \approx h/2e^2$), and being separated by an island formed of a material having a non-uniform density of energy states is proposed. The use of low resistance tunnel junctions is in contrast to the approach used in single electron transistors and the like. In essence, by eschewing the Coulomb blockade approach , the present circuit is able to operate at room temperatures without the severe size restrictions imposed on Coulomb blockade devices. Furthermore, the present circuit differs from resonant tunneling transistors (RTTs) and similar devices, which rely on quantum wells to set the energy scale of the device for its operation. Although the present device is discussed with reference to certain illustrated embodiments thereof, upon review of this specification those of ordinary skill in the art will recognize that the present circuit may be constructed in a number of ways and may find application in a variety of systems. Therefore, in the following description the illustrated embodiments should be regarded as exemplary only and should not be deemed to be limiting in scope.

More precisely, the present transistor includes an island made of material having a band gap. The island is preferably sufficiently large such that electron energy states thereinare separated by less than 100 meV (i.e., energy states in the valence or conduction band, not the band gap). Therefore, at room temperature, the valence and conduction bands of the island behave as continuous energy bands. The island may be regarded as a region that is not connected by Ohmic conduction paths to any other region of the transistor. Metallic leads may be used for source and drain electrodes, and a gate electrode may be capacitively coupled to the island. The tunnel junctions may be formed at the interconnections of tunnel junction barriers disposed between the island and the source and drain electrodes and these tunnel junction barriers may be formed of an insulating material. As indicated above, the tunnel

junctions have a resistance less than a quantum resistance, e.g., less than 26 KOhms. This is possible because the present transistor does not rely on a Coulomb blockade to achieve switching behavior.

Figure 1 shows one embodiment of the present transistor. An insulating layer **22** (e.g., SiO_2) of thickness **40** is disposed on a substrate **20**. The substrate may be made of an appropriate semiconductor material, silicon, for example. Thus, layer **22** may be grown by wet or dry oxidation as is common in the semiconductor processing arts. A gate electrode **24** is located between the substrate **20** and layer **22**.

An island **26** is located on top of the layer **22** and is aligned opposite the gate **24**, so that the gate and the island are capacitively coupled. The island can have a wide range of doping levels, including no doping at all. A source contact **28** and a drain contact **30** are provided at opposite sides of the island **26**, and a thin, insulating film **32** forms a first tunnel junction **34** between the source **28** and the island **26**. Film **32** also forms a second tunnel junction **36** between the drain **30** and island **26**. First tunnel junction **34** (i.e., the film 32 at the point of the first tunnel junction) has thickness **35**, and second tunnel junction **36** (i.e., the film 32 at the point of the second tunnel junction) has thickness **37**. Thicknesses **35**, **37** are determined by the thickness of film **32**. Note, the film 32 may be formed from a material of which island 26 is made (e.g., an oxide thereof), of which source and drain contacts 28 and 30 are made (e.g., an oxide thereof) or of a different material all together.

The source contact **28** and drain contact **30** are preferably made of a metal such as aluminum, copper, gold, titanium or the like. Source and drain contacts made of metal are preferred because metals have higher carrier mobilities. Therefore, metal source and drain contacts provide superior high frequency performance and switching and low power characteristics (e.g., over contacts formed of other materials, such as semiconductors).

It is noted that the apparatus of **Figure 1** is symmetrical; that is, source **28** and drain **30** are interchangeable and tunnel junctions **34** and **36** are also interchangeable. Most

embodiments of the present transistor are symmetrical. However, in some embodiments of the present transistor, first and second junctions **34** and **36** are not identical, and, therefore, in these embodiments the apparatus is not symmetrical.

Film **32** is preferably very thin so that tunnel junctions **34** and **36** have relatively low resistances. For example, film **32** may be 1-40 Angstroms thick. Film **32** may be formed by a chemical vapor deposition (CVD) process, or by oxidizing the island material, for example. Of course, other manufacturing processes may be used, depending on the material of which film 32 is made. In the figure, film **32** is shown to cover the entire island **26**, however, in other embodiments film **32** may cover the island only in regions close to the tunnel junctions **34** and **36**.

Island **26** is made of a material having a band gap, such as silicon, germanium or any other semiconductor material. Island **26** can also be made of superconductor materials, which have a band gap when cooled below a critical temperature. Island **26** is not made of metal. Preferably, island **26** is made of doped (or undoped) semiconductor material. Thus, embodiments of present transistor include p-type and n-type devices having p- and n- doped semiconductor islands.

Tunnel junctions **34** and **36** each have a resistance less than the quantum resistance (e.g., approximately 26 KOhms). The resistance of the first tunnel junction **34** is determined by the thickness **35**, and a surface area of contact (i.e., the junction area) of film 32 between the source **28** and island **26**. The resistance of the second tunnel junction **36** is determined by the thickness **37**, and a surface area of contact of film 32 between the drain **30** and island **26**. The resistance of the tunnel junctions **34**, **36** scales linearly with junction area (lower resistance for larger junction area), and exponentially with thickness (lower resistance for thinner junctions). The tables below provide exemplary (and approximate) thicknesses and junction areas for tunnel junctions having different resistances:

For 26 K-Ohm Tunnel Junctions

Junction Area	Film Thickness
50nm x 50nm	12 Angstroms
100nm x 100nm	18 Angstroms
200nm x 200nm	24 Angstroms

For 13 K-Ohm Tunnel Junctions

Junction Area	Film Thickness
50nm x 50nm	9 Angstroms
100nm x 100nm	15 Angstroms
200nm x 200nm	21 Angstroms

For 2.6 K-Ohm Tunnel Junctions

Junction Area	Film Thickness
50nm x 50nm	2 Angstroms
100nm x 100nm	8 Angstroms
200nm x 200nm	14 Angstroms

More preferably, the tunnel junctions **34** and **36** each have a resistance less than 10 KOhms, and most preferably less than 1000 Ohms. These resistance values are achieved by appropriately selecting the thickness and junction area of film 32 in the area of the tunnel junctions **34** and **36**. It will be apparent to one of ordinary skill in the art that many different combinations of junction thickness and junction area provide junction resistance less than the quantum resistance.

Gate **24** is capacitively coupled to island **26** through layer **22**. Thickness **40** is thick enough so that a resistance between gate **24** and island **26** is very high, such that it essentially

draws no current. For example, this resistance may be on the order of 10^8 Ohms or greater, more preferably, on the order of 10^{10} - 10^{12} Ohms, or greater. Because gate **24** and island **26** are only capacitively coupled, essentially no tunnel current or Ohmic current can flow between the gate **24** and island **26**.

Figure 2 shows a schematic band diagram for an n-type device with no voltages applied to the source **28**, drain **30** or gate **24**. In this embodiment the island **26** is made of n-doped semiconductor material. Source **28** and drain **30** are metals and so have well defined Fermi energies **42s** and **42d**, respectively. Island **26** has a Fermi energy **43**. Island **26** has bandgap **52,** which is on the order of 0.5-3 electron volts, for example. Tunnel junctions **34** and **36** (i.e., the tunnel junction barriers disposed between the source/drain and the island) are made of an insulating material and so have large band gaps **50** compared to island **26**. Also shown is an island conduction band **54**, and an island valence band **56**. Since island **26** is made of n-doped semiconductor material, valence band **56** is completely full, and conduction band **54** is partially full. Also, island Fermi energy **43** is relatively close to conduction band **54**, and donor levels **45** are present just below the conduction band edge.

Conduction band **54** and valence band **56** have many electron energy levels **58** indicated by horizontal lines. As is known in the art, a spacing between the energy levels **58** is dependent upon the size of the island **26** and the material comprising the island. In the present transistor, the island **26** is designed so that the energy levels **58** are separated in energy by less than about 100 meV, more preferably, less than 50meV and most preferably less than 25 meV. This is preferred in the present transistor because it assures that, at room temperature, the valence and conduction bands behave as approximately continuous bands. This is because at room temperature (i.e., where T is approximately 300K) K_bT~25meV, where K_b is Boltzmann's constant. In other words, if the energy levels **58** are spaced apart by less than 25-100meV, electrons at room temperature have enough thermal energy to travel between energy levels **58**.

Figure 3 shows an electrical schematic illustrating how (in one embodiment) the present transistor is used in an electrical circuit. Source **28**, drain **30**, island **26**, and tunnel junctions **34**, **36** are indicated. Capacitor **60** represents capacitance between gate **24** and island **26**. A bias voltage supply V_b **61** provides a voltage between source **28** and drain **30**. The bias supply can provide voltage of both polarities to the source and drain. A gate voltage supply V_g **62** provides voltage between gate **24** and drain. Gate voltage supply **62** can provide both positive and negative voltage to gate **24** with respect to drain **30**.

Figure 4 shows a band diagram of an n-type device while the bias supply **61** applies a small negative voltage to the source **28** with respect to the drain **30**. Gate voltage V_g is zero (i.e., gate **24** and drain **30** are at the same voltage). Voltage **55** across first tunnel junction **34** is not equal to voltage **57** across second tunnel junction **36** due in part to different junction capacitances. More generally, relative voltages across the tunnel junctions **34** and **36** depend upon the relative capacitances between source **28**, island **26**, drain **30** and gate **24**. Also, the different voltages across tunnel junctions **34** and **36** are due to the fact that gate **24** is at the same voltage as drain **30**.

Current does not tunnel between source **28** and drain **30** because the bottom edge of conduction band **54** is higher in energy than the source Fermi energy. Therefore, electrons at the source Fermi energy **42s** cannot tunnel to energy levels **58** in the conduction band **54**. Also, electrons in the valence band **56** cannot tunnel to energy levels at the drain Fermi energy **42d**.

Figure 5 shows a band diagram of the device while the bias supply **58** applies a bias voltage just sufficient to cause conduction. Again, gate voltage V_g is zero. The bias voltage applied in **Figure 5** is greater than the bias voltage applied in **Figure 4**. The bias voltage necessary for conduction (with no gate voltage applied) is the voltage which causes the source Fermi energy **42s** to align with the conduction band **54**/or donor levels **45**. Electrons at the Fermi energy E_f in the source **28** tunnel **64** to the conduction band **54**, and then tunnel **66** from

the conduction band to the drain. The electrons arrive in the drain as hot electrons above the drain Fermi energy **42d**. Again, voltages across tunnel junctions **34** and **36** are shown as unequal, possibly due to differences in relative capacitances, as well as the fact that gate **24** and drain **30** are at the same voltage. It is noted that voltages across junctions **34** and **36** can be equal or unequal in the present transistor.

Figure 6 shows a bandgap diagram of the n-type device with a positive voltage applied to the gate **24** with respect to drain **30**. The conduction band **54** is lowered in energy so that it aligns with the source and drain Fermi energies **42s** and **42d**. Therefore, when a small negative voltage is applied to source **28** with respect to drain **30**, electrons can tunnel from source **28**, to island **26**, to drain **30**. Alternatively, a negative voltage applied to drain **30** will cause electrons to tunnel from drain **30**, to island **26**, to source **28**. Therefore, a sufficiently positive bias applied to gate **24** with respect to the drain **30** allows the device to conduct current in both directions.

To summarize, in the case where the island **26** is made of n-doped semiconductor material, application of a positive gate voltage V_g reduces the bias voltage V_b necessary to allow conduction. Conversely, for n-doped devices, a negative gate voltage V_g increases the bias voltage V_b necessary to cause conduction.

Figure 7 shows a plot of bias voltage (i.e., voltage between source **28** and drain **30**) versus drain current for different values of gate voltage V_g. The plot of **Figure 7** is for a device with an n-doped semiconductor island **26**. V_d represents drain voltage, and V_s represents source voltage. A threshold bias voltage **70** is the bias voltage for which the source Fermi energy **42s** is aligned with the bottom edge of the conduction band **54**. The energy band diagram of **Figure 5** corresponds approximately to the threshold **70**.

A complementary threshold bias voltage **72** represents the bias voltage for cases where a negative voltage is applied to drain. The threshold bias **70** and complementary threshold bias

72 do not necessarily have the same voltage magnitude. Thresholds **70** and **72** are defined for zero gate voltage.

It is noted that the threshold bias voltages **70** and **72** depend in part upon the band gap **52** of the island **26**. If the band gap energy **52** is high (e.g., 4-5 electron volts), then the threshold bias voltages **70** and **72** will be relatively high. If the band gap energy is low (e.g. 0.2-1.5 electron volts), then the threshold bias voltages **70** and **72** will be relatively low.

Also, threshold bias voltages **70** and **72** depend upon the doping level of the island **26**. If the island is highly doped, then threshold bias voltages will be relatively low; if the island is lightly doped, then threshold bias voltages will be relatively high.

The threshold bias voltages **70** and **72** also depend upon the relative capacitances of tunnel junctions **34** and **36**. Consider, for example, a case when source **28** is negative with respect to drain **30** and first tunnel junction **34** has a relativel low capacitance. A voltage applied between source **28** and drain **30** will mostly be across the first tunnel junction **34**. Therefore, only a relatively low voltage is required to align source Fermi energy **42s** and conduction band **56**. That is, threshold voltage **70** will be relatively low. Complementary threshold voltage **72** will be relatively high. Most generally, differences between the first and second tunnel junction characteristics result in differences in threshold bias voltage **70** and complementary threshold bias voltage **72**.

Figure 8 shows an embodiment of the present transistor in which the island is p-doped, i.e., a 'p-type' device. The conduction band **54** and valence band **56** are shifted up in energy compared to the device of **Figure 2**, which has an n-doped island **26**. The p-doped island **26** in **Figure 8** has acceptor states **78** slightly above the valence band edge. The p-type device will conduct between source **28** and drain **30** when the valence band **56** is aligned with the source Fermi energy **42s** or drain Fermi energy **42d**.

Figure 9 shows a p-type device with a negative gate voltage applied. The valence band **56** and acceptor states **78** are raised in energy and aligned with the source Fermi energy **42s**

and drain Fermi energy **42d**. When a negative voltage is applied to the source **28** with respect to drain **30**, electrons tunnel **80** between the source **28**, island **26** and drain **30**. Alternatively, a negative voltage is applied to drain **30** with respect to source 28. Of course, it should be remembered that island 26 may be undoped.

It will be clear to one of ordinary skill in the art that the above embodiments may be altered in many ways without departing from the broader scope of the present invention. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.

CLAIMS

What is claimed is:

1. An apparatus for switching electrical current, comprising:

a) an ohmically isolated island comprised of material having a band gap, wherein the island is sufficiently large such that electron energy levels within the island are separated by less than 100 meV;

b) a source contact;

c) a first tunnel junction barrier disposed between the island and the source contact, wherein the first tunnel junction barrier has a thickness and cross sectional area selected such that a first tunnel junction formed by the source contact, the first tunnel junction barrier and the island has a resistance less than a quantum resistance;

d) a drain contact;

e) a second tunnel junction barrier disposed between the island and the drain contact, wherein the second tunnel junction barrier has a thickness and cross sectional area selected such that a second tunnel junction formed by the drain contact, the second tunnel junction barrier and the island has a resistance less than the quantum resistance;

f) a gate electrode capacitively coupled to the island.

2. The apparatus of claim 1 wherein the island comprises semiconductor material selected from the group consisting of silicon and germanium.

3. The apparatus of claim 1 wherein the first tunnel junction and second tunnel junction each have resistances less than 10 KOhms.

4. The apparatus of claim 1 wherein the first tunnel junction and second tunnel junction each have resistances less than 1 KOhms.

5. The apparatus of claim 1 wherein the first tunnel junction and second tunnel junction each have resistances less than 100 Ohms.

6. The apparatus of claim 1 wherein the first tunnel junction barrier and second tunnel junction barrier each have a thickness less than 24 Angstroms and a cross sectional area greater than 0.04 microns^2.

7. The apparatus of claim 1 wherein the first tunnel junction barrier and second tunnel junction barrier each have a thickness less than 18 Angstroms and a cross sectional area greater than 0.01 microns^2.

8. The apparatus of claim 1 wherein the first tunnel junction barrier and second tunnel junction barrier each have a thickness less than 12 Angstroms and a cross sectional area greater than 0.0025 microns^2.

9. The apparatus of claim 1 wherein the first and second tunnel junction barriers comprise insulator material selected from the group consisting of silicon oxide and aluminum oxide

10. The apparatus of claim 1 further comprising a gate insulating layer disposed between the gate electrode and the island.

11. The apparatus of claim 10 wherein a channel length between the first tunnel junction and second tunnel junction is in the range of 0.02-0.2 microns.

12. A circuit, comprising:

a pair of tunnel junctions, each having a resistance less than or equal to approximately a quantum resistance, separated by an island formed of a material having a non-uniform density of energy states, each of the tunnel junctions being formed by the interconnection of the island with a respective one of a pair of conductors through a tunnel junction barrier; and

a gate electrode capacitively coupled to the island.

13. The circuit of claim 12 wherein the island is formed of a superconductor material.

14. The circuit of claim 12 wherein the island is formed of a semiconductor material.

15. The circuit of claim 14 wherein the semiconductor material comprises silicon.

16. The circuit of claim 14 wherein the semiconductor material comprises germanium.

17. The circuit of claim 12 wherein the tunnel junction barriers are formed of an oxide of a material from which the conductors are made.

18. The circuit of claim 17 wherein the gate electrode is made of the same material as the conductors.

19. The circuit of claim 12 wherein the tunnel junction barriers are formed of an oxide of a material from which the island is made.

20. The circuit of claim 12 wherein the tunnel junction barriers are formed of a material different from that of which the island is made and different from that of which the conductors are made.

21. The circuit of claim 12 wherein the island is formed of an undoped material.

22. The circuit of claim 12 wherein the non-uniform density of energy states comprises at least one region that contains available energy states adjacent to at least one region that does not contain any available energy states.

23. A method, comprising forming a conduction path between a pair of tunnel junctions each having a resistance less than or equal to approximately a quantum resistance by shifting energy states of an island formed of a material having a non-uniform density of such energy states, the island being disposed between the tunnel junctions.

24. The method of claim 23 wherein the energy states of the island are shifted by application or removal of a voltage through an electrode capacitively coupled to the island.

25. The method of claim 24 further comprising passing a current through the conduction path via electrodes coupled to the tunnel junctions.

ABSTRACT

A transistor operated by changing the electrostatic potential of an island disposed between two tunnel junctions. The transistor has an island of material which has a band gap (e.g. semiconductor material). Source and drain contacts are provided. The transistor has a first tunnel junction barrier disposed between island and source, and a second tunnel junction barrier disposed between island and drain. The island is Ohmically isolated from other parts of the transistor as well as a substrate. A gate electrode is capacitively coupled to the island so that a voltage applied to the gate can change the potential of the island. The transistor has n- and p-type embodiments. In operation, applying a gate voltage lowers (e.g., for positive gate bias) or raises (e.g., for negative gate bias) the conduction band and valence band of the island. When the conduction band or valence band aligns with the Fermi energy of the source and drain, tunneling current can pass between the source, island and drain.

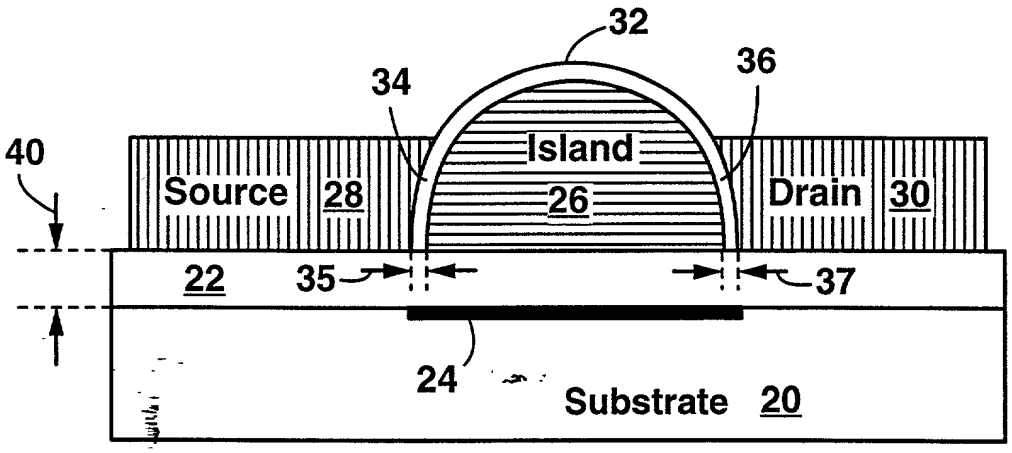
32
34
36
40
Island
26
Source 28
Drain 30
22
35
37
24
Substrate 20

Fig. 1

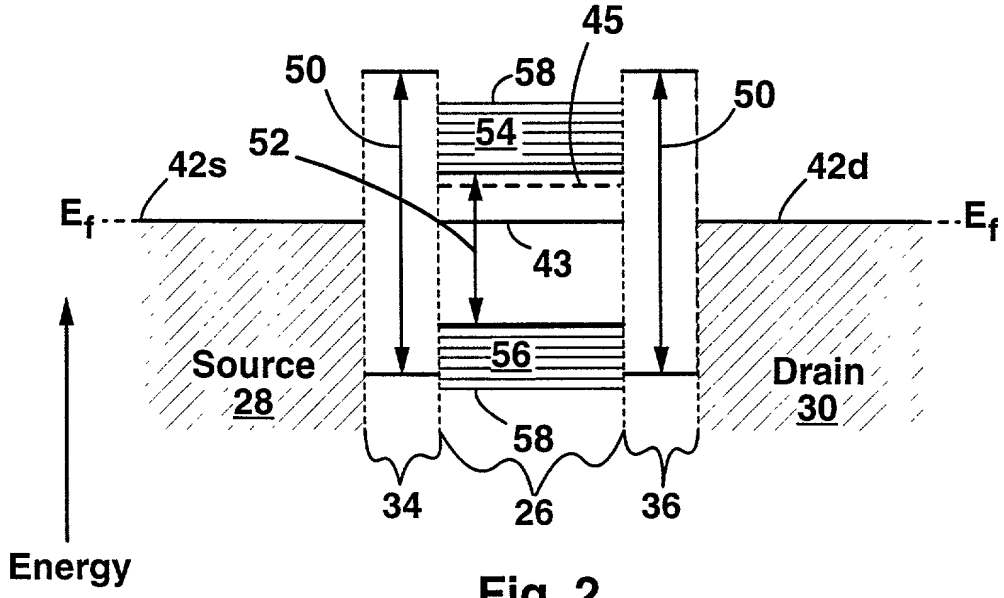
45
50
58
50
54
52
42s
42d
E_f
E_f
43
56
Source
28
Drain
30
58
34
26
36
Energy

Fig. 2

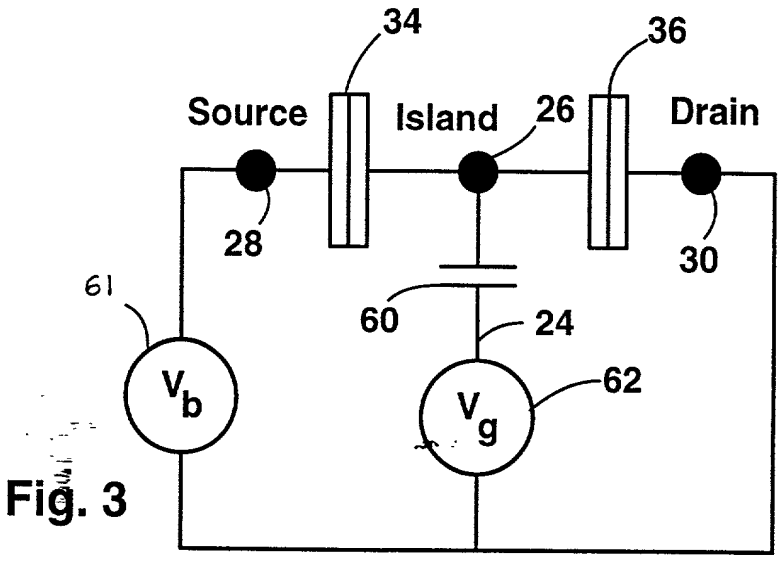
34
36
Source
Island
26
Drain
28
30
61
60
24
V_b
V_g
62

Fig. 3

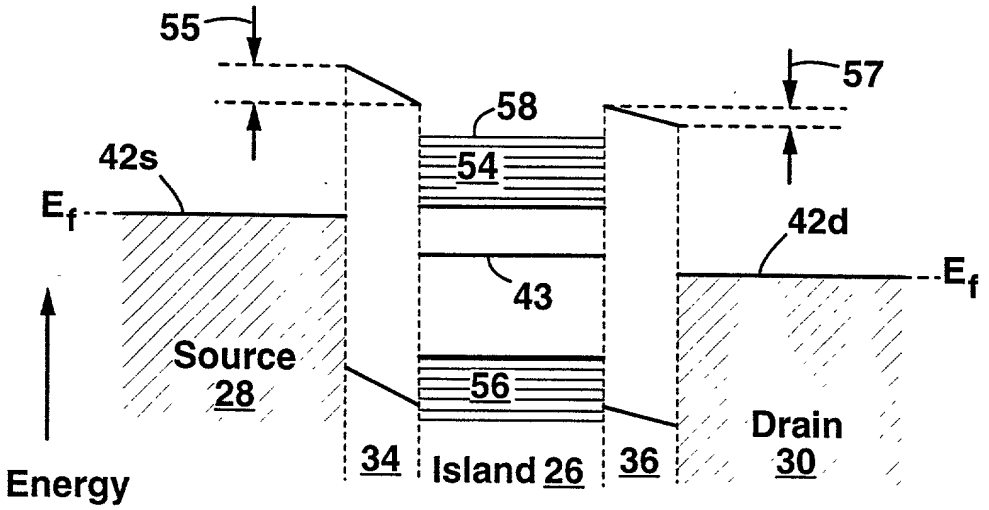
55
57
58
54
42s
E_f
42d
E_f
43
Source
28
56
Drain
30
34
Island 26
36
Energy

Fig. 4

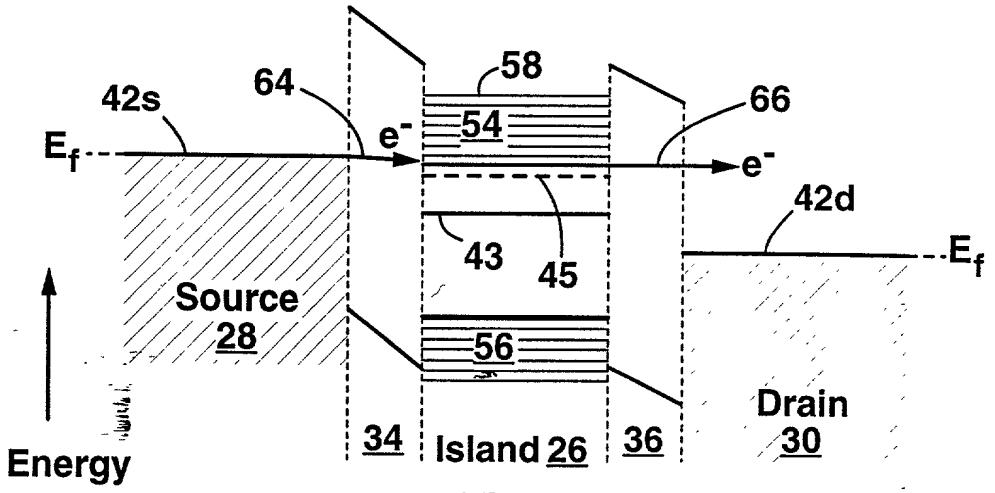
42s
64
58
66
E_f
e^-
54
e^-
42d
43
45
E_f
Source
28
56
Drain
30
Energy
34
Island 26
36

Fig. 5

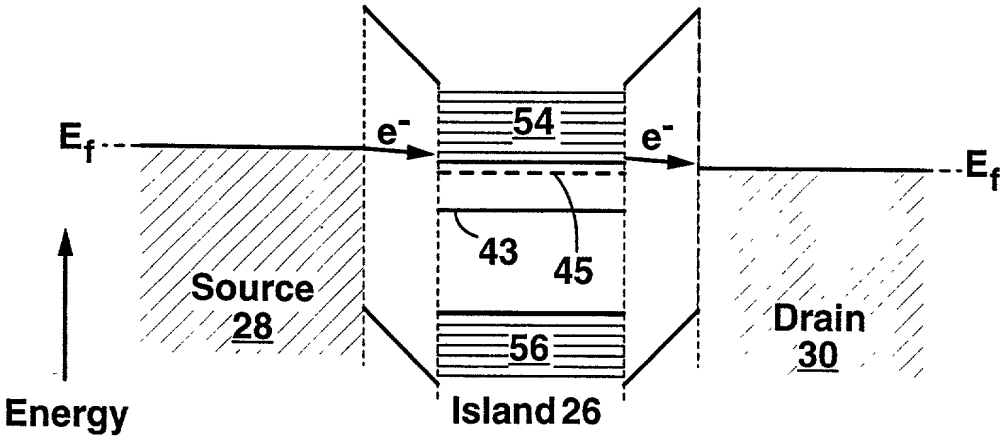
E_f
e^-
54
e^-
E_f
43
45
Source
28
56
Drain
30
Energy
Island 26

Fig. 6

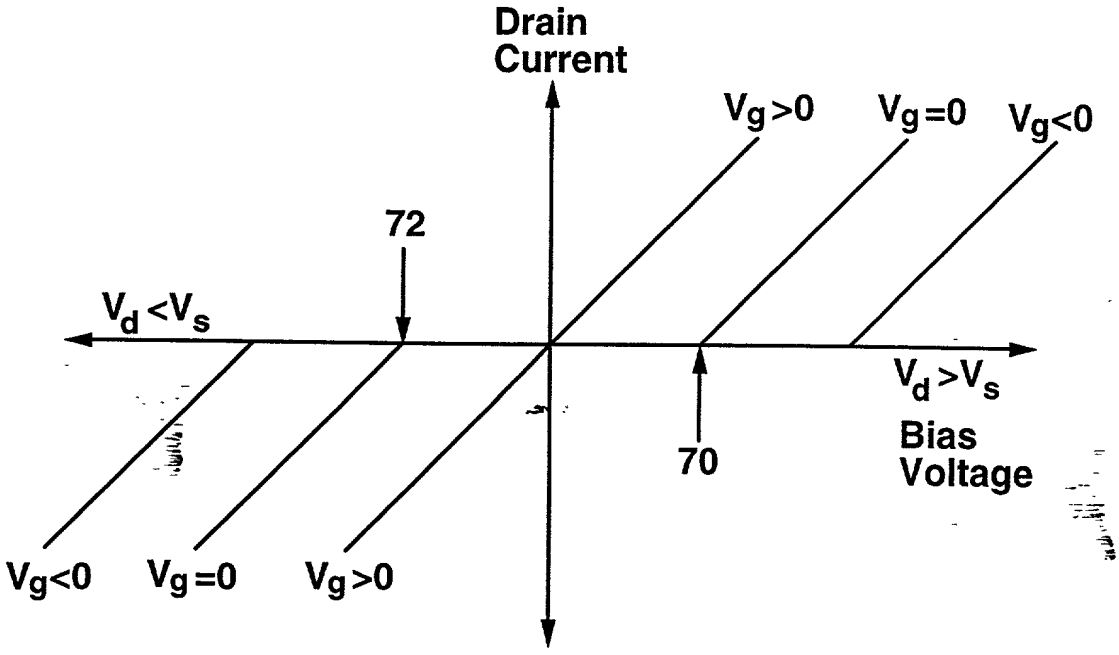
Drain
Current
$V_g>0$
$V_g=0$
$V_g<0$
72
$V_d<V_s$
$V_d>V_s$
70
Bias
Voltage
$V_g<0$
$V_g=0$
$V_g>0$

Fig. 7

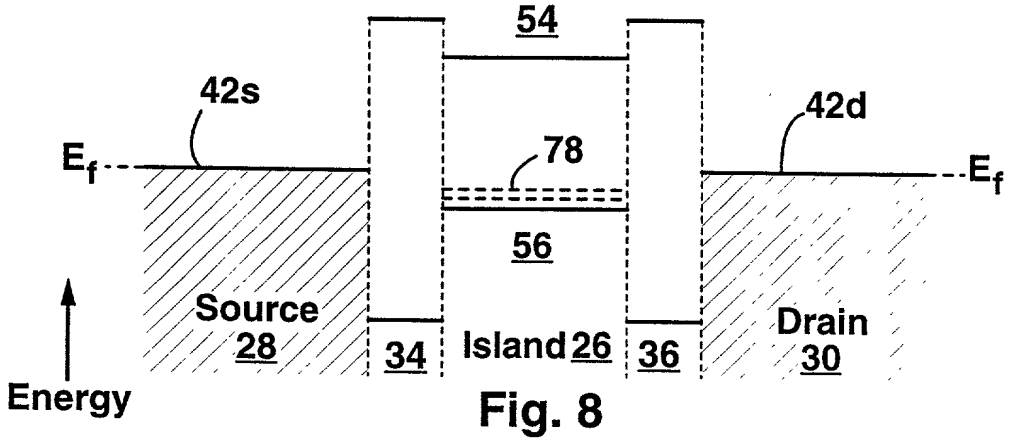
54
42s
42d
E_f
78
E_f
56
Source
28
34
Island 26
36
Drain
30
Energy

Fig. 8

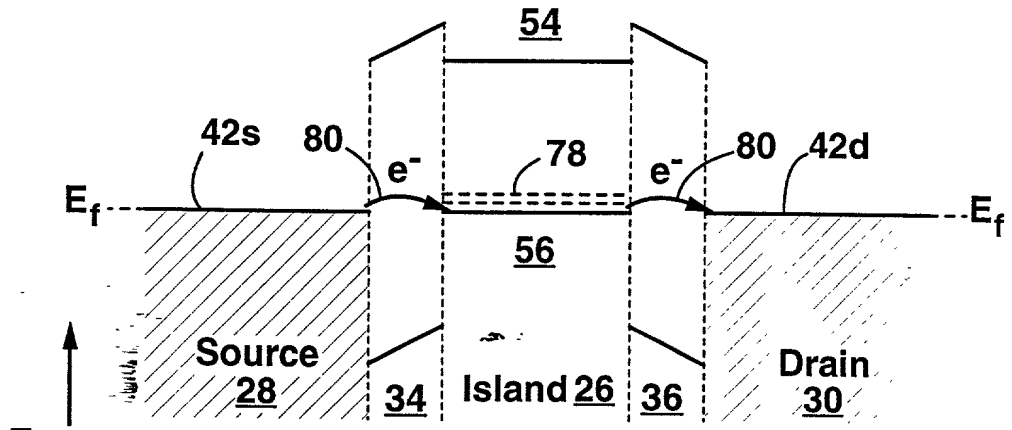
54
42s
80
e-
78
e-
80
42d
Ef
Ef
56
Source
28
34
Island 26
36
Drain
30
Energy

Fig. 9

Attorney's Docket No.: 003771.P001 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTORSTATICALLY OPERATED TUNNELING TRANSISTOR

the specification of which

_X_ is attached hereto.

___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send all correspondence to Tarek N. Fahmi, Reg. No. 41,402, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (408) 720-8598.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Full Name of Sole/First Inventor Daniel E. Grupp

Inventor's Signature _____ Date 4/17/99

Residence Stockton, New Jersey (City, State) Citizenship U.S.A. (Country)

Post Office Address 103 Queen Road, Stockton, NJ 08559

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by ¤¤1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.